Remarks

Reconsideration of this Application is respectfully requested.

Upon entry of the foregoing amendment, claims 8-12, 14-18 and 20-42 are pending in the application, with claims 8, 14, 30, 36, 38 and 41 being the independent claims. Claims 1-7, 13 and 19 were previously cancelled.

Based on the following remarks, Applicants respectfully request that the Examiner reconsider all outstanding objections and rejections and that they be withdrawn.

Rejections under 35 U.S.C. § 103

Claims 8-12, 14-18, 25-29

The Examiner has rejected claims 8-12, 14-18 and 25-29 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,488,729 to Vegesna *et al.* ("Vegesna") in view of U.S. Patent No. 5,481,734 to Yoshida ("Yoshida"). For the reasons set forth below, Applicants respectfully traverse.

Independent claim 8 is directed to a superscalar microprocessor for processing instructions. Among other features, the microprocessor of claim 8 includes "a branch prediction circuit configured to provide a branch bias signal indicating whether a conditional branch controlled by a conditional branch instruction is predicted to be taken or not taken" and "an instruction buffer . . . configured to buffer a plurality of fetched instructions, including an instruction selected according to the branch bias signal."

In support of the rejection of claim 8, the Examiner asserts that the foregoing features are taught by Vegesna. Applicants respectfully disagree. Vegesna describes a

CPU architecture that does not use branch prediction. Rather, in Vegesna's architecture, a branch instruction is handled by testing the condition associated with the branch instruction during the decode stage of the processor pipeline and then fetching a target instruction based on the actual results of the condition:

> As previously discussed, the branch is decoded and executed during the (D) pipestage. The PCU (6, FIG. 18) calculates the effective address of the target using the address of the branch instruction itself and the offset value specified in the imm22 bit field of the instruction. . . . The condition codes are evaluated by the PCU (6, FIG. 19) and the delay slot instruction fetch is also initiated during (D). During the (E) pipestage, the target instruction is fetched if the branch is to be taken, otherwise the next sequential instruction after the dsi is fetched.

Vegesna, column 25, lines 55-67.

In fact, Vegesna only mentions branch prediction in a section describing prior art approaches. Yet, in that section, Vegesna merely describes one system that always predicts that the branch will not be taken (*see* Vegesna, column 10, line 66-column 11, line 15) and another system that always predicts that the branch will be taken (*see* Vegesna, column 11, lines 16-25), but nowhere describes a system that includes a "branch prediction circuit configured to provide a branch bias signal indicating whether a conditional branch controlled by a conditional branch instruction *is predicted to be taken or not taken*" as recited by claim 8. Furthermore, since Vegesna does not teach or suggest a branch prediction circuit that provides a branch bias signal as recited in claim 8, it also cannot teach or suggest "an instruction buffer . . . configured to buffer a plurality of fetched instructions, including an instruction selected according to the branch bias signal" as recited by the claim.

The foregoing deficiencies of Vegesna with respect to independent claim 8 are in no way remedied by the teachings of Yoshida. Consequently, the combination of

Vegesna and Yoshida cannot render obvious independent claim 8. Dependent claims 9-12, 25 and 26 are likewise not rendered obvious by the combination of Vegesna and Yoshida for the same reasons as independent claim 8 from which they depend and further in view of their own respective features. Accordingly, Applicants respectfully request that the rejection of claims 8-12, 25 and 26 under 35 U.S.C. § 103(a) be reconsidered and withdrawn.

Independent claim 14 is directed to a method for processing instructions in a superscalar microprocessor. Among other features, the method of claim 14 includes "predicting whether a conditional branch controlled by a conditional branch instruction included in the fetched instructions is taken or not taken" and "buffering a plurality of fetched instructions, including an instruction selected according to the prediction, in an instruction buffer." For reasons set forth above with respect to claim 8, neither Vegesna nor Yoshida teach or suggest these features. Thus, the combination of Vegesna and Yoshida cannot render obvious independent claim 14. Dependent claims 15-18 and 27-29 are likewise not rendered obvious by the combination of Vegesna and Yoshida for the same reasons as independent claim 14 from which they depend and further in view of their own respective features. Accordingly, Applicants respectfully request that the rejection of claims 14-18 and 27-29 under 35 U.S.C. § 103(a) be reconsidered and withdrawn.

Claims 20-24

The Examiner has rejected claims 20-24 under 35 U.S.C. § 103(a) as being unpatentable over Vegesna in view of Yoshida as applied to independent claims 8 and 14 and further in view of U.S. Patent No. 5,446,912 to Colwell *et al.* ("Colwell"). However,

Colwell is not prior art with respect to the claims of the present application. In particular, the earliest effective filing date of Colwell is September 30, 1993, while the earliest effective filing date of the present application is July 8, 1991. Consequently, the rejection of claims 20-24 over the combination of Vegesna, Yoshida and Colwell is improper and Applicants respectfully request that it be reconsidered and withdrawn.

Claims 30-41

The Examiner has rejected claims 30-41 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 4,942,525 to Shintani *et al.* ("Shintani") in view of U.S. Patent No. 4,594,655 to Hao *et al.* ("Hao"). For the reasons set forth below, Applicants respectfully traverse.

Independent claim 30 is directed to a method of executing instructions using a microprocessor. Among other features, claim 30 includes "pre-fetching an instruction group including a plurality of instructions from a memory in a first processor cycle and holding the instruction group in a pre-fetch buffer, the pre-fetching accomplished so that instruction groups can be returned out of program order and subsequently reordered."

In support of the rejection of independent claim 30, the Examiner asserts that Shintani teaches the foregoing feature. Applicants respectfully disagree. Shintani describes a data processor that facilitates concurrent execution of instructions by a plurality of functional units. Shintani's data processor includes an instruction fetch circuit 201 that fetches instructions from a memory 1 into one of two prefetch instruction buffers 202 or 203. However, Shintani nowhere teaches or suggests that the instructions can be returned from memory 1 "out of program order and subsequently reordered" as recited by independent claim 30.

The Examiner has cited to the text at column 7, lines 32-42 of Shintani as teaching the reordering of instructions fetched from memory out of program order. However, the language cited by the Examiner relates to an output exchange circuit 9 that receives output data from a plurality of execution units and rearranges the output for provision on a plurality of "set-up ports". Thus, the text cited by the Examiner relates to the distribution of execution results, not to the reordering of instructions fetched from memory out of program order.

The foregoing deficiencies of Shintani with respect to independent claim 30 are in no way remedied by the teachings of Hao. Consequently, the combination of Shintani and Hao cannot render obvious independent claim 30. Dependent claims 31-35 are likewise not rendered obvious by the combination of Shintani and Hao for the same reasons as independent claim 30 from which they depend and further in view of their own respective features. Accordingly, Applicants respectfully request that the rejection of claims 30-35 under 35 U.S.C. § 103(a) be reconsidered and withdrawn.

Independent claim 36 is directed to a data processing apparatus comprising a superscalar type microprocessor having a plurality of functional units that can execute instructions simultaneously. Among other features, the microprocessor of claim 36 includes "a buffer that buffers a plurality of instruction groups pre-fetched by the pre-fetch unit . . . wherein when a plurality of instructions of the instruction group are all retired, an entry in the buffer corresponding to the instruction group is released."

These features of independent claim 36 are not taught or suggested by Shintani. As discussed above, Shintani teaches a data processor that includes an instruction fetch circuit 201 that fetches instructions from a memory 1 into one of two prefetch instruction

buffers 202 or 203. However, Shintani does not teach or suggest that instructions are stored in the buffers as "a plurality of instruction groups" as recited by independent claim 36. Furthermore, although Shintani does state that instructions are "extracted" from the instruction buffers 202 and 203 by instruction fetch circuit 201, Shintani nowhere teaches or suggests that when a plurality of instructions of an instruction group are retired, an entry in the buffer corresponding to the instruction group is released as recited by independent claim 36.

The foregoing deficiencies of Shintani with respect to independent claim 36 are in no way remedied by the teachings of Hao. Consequently, the combination of Shintani and Hao cannot render obvious independent claim 36. Dependent claim 37 is likewise not rendered obvious by the combination of Shintani and Hao for the same reasons as independent claim 36 from which it depends and further in view of its own respective features. Accordingly, Applicants respectfully request that the rejection of claims 36 and 37 under 35 U.S.C. § 103(a) be reconsidered and withdrawn.

Independent claim 38 is directed to a data processing apparatus comprising a superscalar type microprocessor having a plurality of functional units that can execute instructions simultaneously. Among other features, the microprocessor of claim 38 includes "a retirement unit that specifies a register in which to store a result of executing [an] instruction outside the predetermined program order". Shintani nowhere teaches or suggests a retirement unit, let alone one that specifies a register in which to store the result of an instruction executed outside the predetermined program order as recited by independent claim 38. The text cited by the Examiner at column 5, line 65-column 6, line 7 of Shintani as teaching this feature relates instead to the execution of a

microprogram associated with an instruction by an ALU control circuit and the generation of an output signal when the execution of the microprogram is complete. Thus, the cited text does not teach or suggest the relevant features.

The foregoing deficiencies of Shintani with respect to independent claim 38 are in no way remedied by the teachings of Hao. Consequently, the combination of Shintani and Hao cannot render obvious independent claim 38. Dependent claims 39-40 are likewise not rendered obvious by the combination of Shintani and Hao for the same reasons as independent claim 38 from which they depend and further in view of their own respective features. Accordingly, Applicants respectfully request that the rejection of claims 38-40 under 35 U.S.C. § 103(a) be reconsidered and withdrawn.

Independent claim 41 is directed to a data processing apparatus comprising a superscalar type microprocessor having a plurality of functional units that can execute instructions simultaneously. Among other features, the microprocessor of claim 41 includes "a buffer having plural stage registers that can transfer stored data in a forward direction and that stores the plurality of instructions of the pre-fetched instruction group" and "an instruction completion unit that advances contents of a plurality of registers of the buffer in the forward direction by a number of stages that correspond to a number of groups of completed instructions."

The Examiner has asserted that these features are taught by Shintani. Applicants respectfully disagree. As discussed above, Shintani teaches a data processor that includes an instruction fetch circuit 201 that fetches instructions from a memory 1 into one of two prefetch instruction buffers 202 or 203. However, Shintani nowhere teaches or suggests that either buffer 202 or 203 has "plural stage registers that can transfer

stored data in a forward direction" as recited by independent claim 41. Furthermore, Shintani nowhere teaches or suggests "an instruction completion unit" that can advance the contents of a plurality of registers of either buffer 202 or 203 in a forward direction by a number of stages that correspond to a number of groups of completed instructions" as recited by that claim.

The foregoing deficiencies of Shintani with respect to independent claim 41 are in no way remedied by the teachings of Hao. Consequently, the combination of Shintani and Hao cannot render obvious independent claim 41. Dependent claim 42 is likewise not rendered obvious by the combination of Shintani and Hao for the same reasons as independent claim 41 from which it depends and further in view of its own respective features. Accordingly, Applicants respectfully request that the rejection of claims 41 and 42 under 35 U.S.C. § 103(a) be reconsidered and withdrawn.

Other Matters

The Examiner has acknowledged receipt of and approved the terminal disclaimers filed in the present application on January 5, 2005. However, the Examiner has stated that "new submissions of the [terminal disclaimer] are required in the continuation case." *See* Office Action at page 1. Applicants respectfully seek clarification from the Examiner regarding this additional requirement. In particular, Applicants seek clarification regarding whether the Examiner is requesting that Applicants file an additional terminal disclaimer in the present application (and if so, with respect to what applications or patents), or whether the Examiner is requesting that

Applicants file a terminal disclaimer in a different application (and if so, which application).

The Examiner notes that a second Information Disclosure Statement (IDS) filed by a different law firm in a different application (U.S. Patent Application 10/781,328) on March 24, 2004 appears to have been associated with the present application by the USPTO. *See* Office Action at page 1. Applicants has viewed this second IDS in PAIR and confirm that this IDS has been associated with the present application in error. Applicants further confirm that Applicants filed a different IDS in the present application on March 24, 2004, citing four references, which the Examiner has already acknowledged.

Conclusion

All of the stated grounds of objection and rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider all presently outstanding objections and rejections and that they be withdrawn. Applicants believe that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment and Reply is respectfully requested.

Respectfully submitted,

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